REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with Markings to Show Changes Made**."

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicant believes that Claims 1-37 are in condition for allowance, and allowance of the application is therefore requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231, on September 9, 2002.

Pat Slaback
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS

11. (Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of:

executing software code for a logic analyzer located within [the] **an** FPGA-based SoC, said software code being the core software code for said logic analyzer utilized for developing and verifying [a] said FPGA-based SoC;

defining at least one monitor probe point within said FPGA-based SoC for analysis by said logic analyzer, wherein the software code and at least one monitor probe point defined [is] are created during customization of [the] said FPGA-based SoC; and

collecting information for said at least one monitor probe point to facilitate analysis of signals while developing and verifying said FPGA-based SoC.

21. (Amended) A FPGA-based SoC development and verification system, the system comprising:

a software core for a logic analyzer inserted within the FPGA-based [embedded processor] SoC during customization of the FPGA-based [embedded processor] SoC;

an external software monitor tool having an interface for communicating with said logic analyzer software core; and

a communication port for facilitating exchange of data between said logic analyzer software core and said external monitor tool.

29. (New) A method for developing and verifying a FPGA-based SoC within a system, the method comprising:

executing software code for a logic analyzer located within the FPGA-based SoC, the software code being the core software code for the logic analyzer;

defining at least one monitor probe point within the FPGA-based SoC for analysis by the logic analyzer, wherein the software code and the at least one monitor probe point defined are created during customization of the FPGA-based SoC; and

collecting information for the at least one monitor probe point to facilitate analysis of signals within the system while developing and verifying the FPGA-based SoC.

30. (New) The method of claim 29, wherein the system further includes a microprocessor coupled to the FPGA-based SoC.

31. (New) The method of claim 29, wherein the FPGA-based SoC is an FPGA-based embedded processor SoC.

32. (New) A machine readable storage having stored thereon, a computer program having a plurality of code sections, the code sections executable by a machine for causing the machine to perform the steps of:

executing software code for a logic analyzer located within an FPGA-based SoC portion of a system, the software code being the core software code for the logic analyzer utilized for developing and verifying the FPGA-based SoC;

defining at least one monitor probe point within the FPGA-based SoC for analysis by the logic analyzer, wherein the software code and at least one monitor probe point defined are created during customization of the FPGA-based SoC; and

collecting information for the at least one monitor probe point to facilitate analysis of signals within the system while developing and verifying the FPGA-based SoC.

33. (New) The machine readable storage of claim 32, wherein the system further includes a microprocessor coupled to the FPGA-based SoC.

34. (New) The machine readable storage of claim 32, wherein the FPGA-based SoC is an FPGA-based embedded processor SoC.

35. (New) A GUI for development and verification of a system including an FPGA-based SoC, the GUI comprising:

a selection dialog for defining and selecting monitor probe points within the system, the monitor probe points being located within the FPGA-based SoC;

a display window for displaying waveforms for trace and trigger conditions; and

a communication interface for facilitating communication with a logic analyzer core integrated within the FPGA-based SoC.

36. (New) The GUI of claim 35, wherein the system further includes a microprocessor coupled to the FPGA-based SoC.

37. (New) The GUI of claim 35, wherein the FPGA-based SoC is an FPGA-based embedded processor SoC.